TOWERJAZZ Design Enablement

www.towerjazz.com

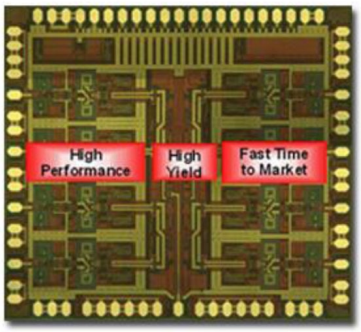
cadence Process Overview

TowerJazz offers wafer foundry services providing the widest range of customizable CMOS specialty processes and proven design enablement tools for the manufacture of optimized integrated circuits (ICs). Our process technologies with geometries ranging from 1.0-to 0.13-micron include: SiGe, BiCMOS, Mixed-Signal & RFCMOS, CMOS Image Sensor (CIS), Power Management (BCD), Digital CMOS, Embedded Non-Volatile Memory (NVM) as well as MEMS capabilities integrated with CMOS. These modular processes are tailored to meet your precise specifications for the most cost-effective and versatile solutions.

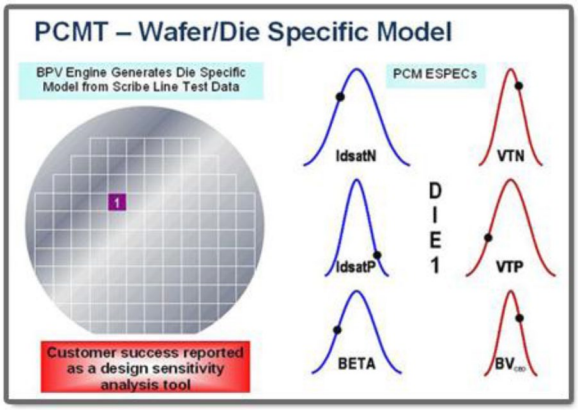
We offer a proven design enablement platform for unprecedented accuracy and first-time success including silicon verified and scalable device models and robust physical design tools. In addition, we offer Transfer Optimization and Process Services (TOPS) to IDMs and fabless companies to expand capacity or provide second sourcing.

TowerJazz PDKs offer a front-to-back integrated custom design environment that supports all major EDA vendors' design flows. Our design kits contain the parameters such as layer thickness and stress gradient that have been well defined within the tolerances of our specific manufacturing processes. The kit automatically sets these constraints for the designer allowing only those parameters to be varied during the evaluation of designs and allowing only those designs that are perfectly compatible with the manufacturing process.

PDK Add-ons that Reduce Time to Market



- **PCMT**: Process Control Monitoring Model Tool that allows you to evaluate wafer or die specific performance in your simulation environment.
- **X-Sigma**: A unique process variation-modeling tool that allows design teams to trade off yield vs. performance and efficiently perform design sensitivity analysis.
- **RMT**: A Reliability Modeling Tool is offered in the Silicon Germanium BiCMOS (SBC) family of technologies, enabling users to predict chip operation as a function of operating conditions and age.
- **JIT**: The Jazz Inductor Toolbox is a searchable inductor database with automated instantiation of schematic and layout of highly optimized inductors. Support of square and octagonal inductors with and without shields is included.
- **PADL**: A pre-characterized Power Amplifier Design Library accelerates SiGe PA design to market through off the shelf power cells and PA-centric technology.
- **Digital Design**: Logic RTL to GDS synthesizable design flow support through industry standard EDA tools.



Process Design Kits Include:

- Symbols and schematics
- Scalable Models with RF accuracy
- Advanced models such as PSP and MOSFETs, HICUM for BJTs, R3 resistors and MOS Model 20 for LDMOS devices
- Monte Carlo Statistical and Mismatch Simulation Capability
- Scalable layout cells (Pcells) with time saving and features targeted for end applications and tightly coupled to the model
- An industry first scalable drift length LDMOS
- Scalable inductors
- Extensive Enhanced Layout Utilities to speed layout cycle time
- Parasitic Extraction and Back-Annotation integrated with model and layout features

TowerJazz PDK			PDK			VXL
Density	**Process**	**Description**	**IC5.1**	**IC6.1**	**Spectre**	**Pcells**
0.35µm	BC35	27/22 Ft BiCMOS with 3.3 or 5.0V	X	–	X	X
0.35µm	SBC35	61/46/23 or 15 Ft SiGe BiCMOS with 3.3 or 5.0V	X	–	X	X
0.25µm	BVD25	HV CMOS with 4/20/40V LDMOS	X	–	X	X
0.25µm	CA25	Digital and RF CMOS with 3.3V	X	–	X	X
0.18µm	SBC18	26.5, 78/38, 155/78/38, 200/75 or 250/100 Ft SiGe BiCMOS with 3.3V, 1.8/3.3 or 1.8/5.0V	X	X	X	X
0.18µm	CA18	0.18µm RF CMOS with 1.8/3.3, 1.8/5.0 or 5.0V	X	Q1'12	X	X
0.13µm	CA13	RF CMOS with 1.2/3.3V	X	X	X	X
0.13µm	SBC13	200 / 75 Ft SiGe BiCMOS with 1.2/3.3V	X	X	X	X
0.13µm	SBL13	90/67/37 Ft SiGe BiCMOS Lite with 1.2/3.3V Al Backend	X	X	X	X
0.13µm	TSBL13	SiGe BiCMOS Lite with 1.2/3.3V with Cu Backend	X	–	X	X
0.13µm	TS13	Digital Logic with 1.2/2.5/3.3V	X	–	X	X
0.13µm	TS13RF	Mixed-Signal with 1.2/3.3/5.0V	X	–	X	X
0.18µm	TS18	Digital Logic with 1.8/3.3/5.0V	X	–	X	X
0.18µm	TS18RF	Mixed-Signal with 1.8/3.3/5.0V	X	–	X	X
0.18µm	TS18IS	CIS1 with 1.8/3.3/5.0V	X	–	X	X
0.18µm	TS18FE	NVM2 with 1.8/3.3/5.0V	X	–	X	X
0.18µm	TS18PM	Power Management with 1.8/5V	X	–	X	X
0.35µm	TS35	Digital Logic with 3.3/5.0V	X	–	–	X
0.35µm	TS35	Mixed-Signal with 3.3/5.0V	X	–	–	X
0.35µm	TS35	CIS with 3.3/5.0V	X	–	–	X
0.35µm	TS35PM	Power Management with 3.3/5.0V	X	–	–	X
0.5µm	TS50	Mixed-Signal with 3.3/5.0V	X	–	–	X
0.5µm	TS50	CIS with 3.3/5.0V	X	–	–	X
0.5µm	TS50	NVM with 3.3/5.0V	X	–	–	X
0.6µm	TS60	Digital Logic with 5V	X	–	–	X