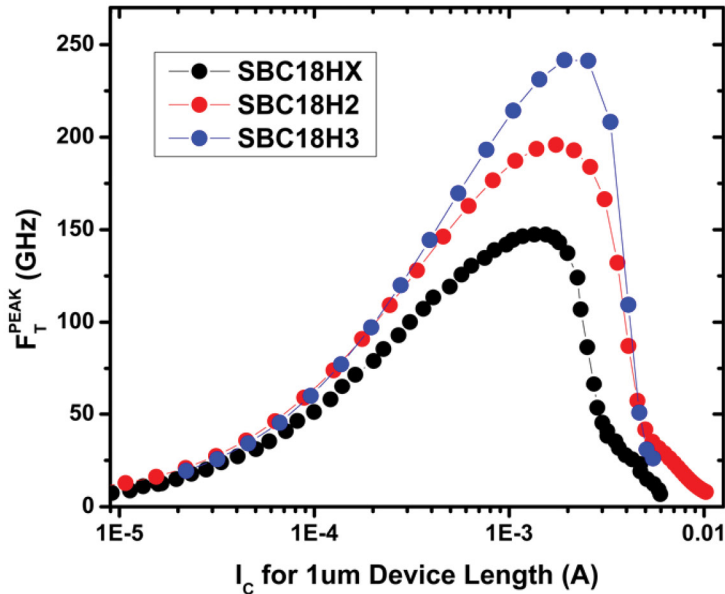


Our industry leading SiGe process is optimized for next-generation needs for high-speed interfaces in communication protocols such as Thunderbolt, optical fiber, and high-data rate wireless by improving performance while reducing noise and power consumption of key building blocks. SBC18H3 also targets applications such as automotive collision avoidance systems, millimeter-wave radar and GHz imaging.

SBC18H3 is TowerJazz's third generation 0.18 μ m SiGe technology and offers transistors with 240GHz Ft and 270GHz Fmax in a cost-effective and analog-friendly 0.18 μ m node. IP of high-speed components such as TIAs, Laser Drivers, SerDes, CDRs from H2 and HX can be readily ported to the new H3 process since they are all in the same 0.18 μ m node while power consumption and noise can be reduced and performance improved.

Power consumption is dramatically reduced with H3 where, for example, a 77GHz amplifier can be made to consume three times less DC power than was possible with older technology. At the same time, noise is improved to levels that far exceed those of prior SiGe technology and are superior to numbers typically reported for more expensive III-V material systems (minimum noise figure at 20GHz is measured at less than 1dB and at 40GHz at only 2dB).

SiGe H3 Technology		
Device	Parameter	SBC18H3
CMOS FET	Nmos (v)	1.8/3.3
	Pmos (v)	1.8/3.3
	Density (μ m)	0.18
BJT	Ft (GHz)	240
	Fmax (GHz)	270
Deep Trench	-	Yes
Schottky Diode	Von (V) @ Ion = 100 μ A	0.41
Triple Well (DNW)	-	Yes
P-I-N Diode	Insertion Loss (dB) @ 50GHz	-3.5
BJT PNP	Lateral PNP	Yes
	Parasitic VPNP	Yes
Capacitors	Stacked MIM CAP (fF/ μ m ²)	4.0
Varactors	High Performance PN Junction, Sensitivity (%/V)	21
	MOS	Yes
Resistors	Unsilicided P + Poly resistor (Ohm/sq)	235 and 1K
	Silicided P + Poly resistor	6
	Metal resistor (Ohm/sq)	24
	Nwell resistor (Ohm/sq)	890
Inductors	-	Yes



Customer Service and Support

- File Exchange for design kits and online documentation
- Online WIP
- Online Tape-Out System
- Online Help Ticket System
- Dedicated Sales and Engineering Support

SiGe Design Kit Features

- Scalable models and p-cells for all devices
- Transmission line toolbox
- Advanced inductor toolbox (JIT)
- Advanced X-sigma corner modeling

Analog Mixed-Signal Design Kit Features

- Cadence®-based Design Kit
- Cadence® Assura™ DRC/LVS/RCX
- Support for Mentor® Calibre interactive/XRC
- Support for Spectre, ADS (& RFDE), HSPICE simulators
- Includes basic ESD structures

ASIC Library Views and Features

- Standard Cell Libraries
- I/O Libraries
- Synopsys and Cadence ASIC Flows
- Memory Generators

Supported Models

- **MOSFETs:** Scalable BSIM/PSP models, RF extension models, mismatch, statistical and noise models
- **NPNs:** HiCUM RF models, mismatch, statistical and noise models
- **MIM Caps:** RF models, mismatch and statistical models
- **Resistors:** Mismatch, statistical and noise models