

The TowerJazz RF CMOS SOI switch process combines a 6 or 4 metal layer CMOS process with a 1000 Ω -cm high resistivity SOI substrate. It is a 0.18 μ m technology with options for 1.8V, 2.5V, 3.3V, and 5V transistors with proven IP for 4T and 6T switches and world class design enablement for higher throw-count switches.

Process options include a low-Vt MOSFET, a 5V RFLDMOS device with Ft of 19 GHz and BVDSS of 20V and passive components including silicided and unsilicided poly resistors, 2 fF/ μ m and stacked 4 fF/ μ m metal-insulator-metal capacitors, scalable geometry inductors and fixed geometry inductors, and fixed geometry baluns and transformers.

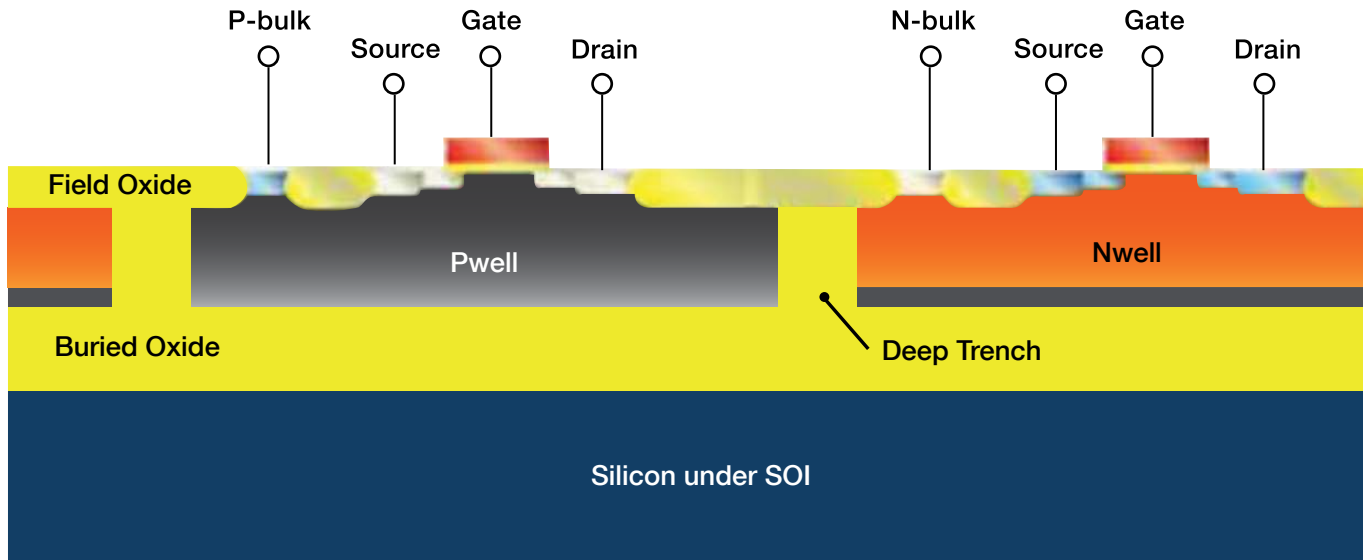
The backend metal is Aluminum with a 2.8 μ m thick top layer for high Q inductors. Substrate options include “thick-film” for bulk-like behavior of the active MOSFETs, free of floating body effects and “thin-film” for the best Ron-Coff performance. Isolation between device wells and of field areas below sensitive passive components and metal routing is provided by an oxide filled deep trench to the buried oxide.

These processes are well-suited for technologies requiring isolation such as cellular switches. Excellent channel isolation better than -40 dBm, insertion loss of 0.47 dB, low harmonics of better than 80dBc at cellular power levels and inter-modulation distortion below -117 dBm have been demonstrated.

RF CMOS SOI Switch Technology

DEVICE	PARAMETER	CA18HB	CA18QC	CS18
CMOS	VDD (V)	1.8/5	1.8/3.3	2.5
	Ron (ohm-mm)	0.68/2.2	0.68/1.6	0.72
	BVdss (V)	> 3.2/8	> 3.2/6	> 3
	Ft (GHz)	55/17	55/26	NA
HV NMOS	Vgs/Vds (V)	5/10	—	—
HV PMOS	Vgs/Vds (V)	5/8	—	—
RFLDMOS	—	Yes	—	—
Native NFET	VDD (V)	5	3.3	—
PDM Deep-trench	—	Yes	Yes	Yes
Resistors	Sheet resistance (ohm/sq.)	6, 310	6, 310, 1000	310, 1000
MiM (Single / Stacked)	Capacitance (fF/ μ m ²)	2/4	2/4	2
Varactors	P+/nwell (fF/ μ m ²)	1.3	1.3	NA
	Mos	Yes	Yes	—
Metal Layers	—	6	4	4
Top Metal	Thickness (μ m)	2.8	2.8	2.8
Substrate	—	1000 ohm-cm + Thick Film SOI	1000 ohm-cm + Thick Film SOI	1000 ohm-cm + Thin Film SOI

RF CMOS SOI Switch Cross Section



0.18 μ m CMOS Design Kit Overview

- Scalable models and p-cells for all devices
- Advanced inductor toolbox (JIT)
- Advanced X-sigma corner modeling
- PCM based models

Analog Mixed-Signal Design Kit Features

- Cadence®-based Design Kit
- Cadence® Assura™ DRC/LVS/RCX
- Support for Mentor® Calibre interactive/XRC
- Support for Spectre, ADS (& RFDE), HSPICE simulators
- Includes basic ESD structures

ASIC Library Views and Features

- Standard Cell Libraries
- I/O Libraries
- Synopsys and Cadence ASIC Flows
- Memory Generators

Supported Models

MOSFETs: Scalable BSIM/PSP models, RF extension models, Non-quasi-static PSP models, mismatch, statistical and noise models

BJTs: Gummel-poon models, mismatch and statistical models

MIM Caps: RF models, mismatch and statistical models

Resistors: Mismatch, statistical and noise models

Varactors: Scalable RF and statistical models

Customer Service and Support

File Exchange for design kits and online documentation

Online WIP

Online Tape-Out System

Online Help Ticket System

Dedicated Sales and Engineering Support